WHAT IS CLAIMED IS :

1. A device to synthesize a frequency F1→F2 with high spectral purity, comprising a synthesizer with a variable step F3→F4, comprising at least one variable rank divider Nb located after said synthesizer and a frequency control device delivering the division rank command of the variable rank divider, the command of the frequency of the variable-step synthesizer, the command of the synthesis step of the variable-step synthesizer.

2. A device according to claim 1 comprising a filtering device positioned after the variable-rank device Nb.

3. A device according to one of the claims 1 or 2, wherein the variable-step synthesizer is a fractional step phase-locked loop synthesizer.

4 . A device according to one of the claims 1 or 2 wherein the variable-rank divider Nb takes the values N1 to Np, these values following an arithmetic progression, and wherein the maximum frequency of the synthesizer is given by F4=N1*F2 where N1 is the smallest value of the sequence and the frequency F3 is a function of N2.

5 . A device according to claim 4 wherein the value of the frequency F3 is substantially equal to or slightly lower than (N1/N2)*F4.

6 . A device according to one of the claims 1 or 2 wherein the variable-rank divider Nb takes the values N1 to Np, these values following a non-arithmetic progression.

7 . A device according to claim 6 wherein F3 is substantially equal to or smaller than aF4 where a is the smallest value obtained in dividing two consecutive elements one after the other.

8 . A device according to claim 6 wherein the highest division rank Nb is chosen.

9 . A device according to claim 1 comprising a mixer receiving the output signal from the fractional step synthesizer and a mixing signal.

10. A method to synthesize a frequency F1→F2 with high spectral purity using a variable-step synthesizer F3→F4, comprising at least one step in which the output signal of the variable-step synthesizer is transmitted to a multiple-rank divider Np and wherein the division rank, the synthesis step of the synthesizer and the frequency of the variable-step synthesizer are modified.

11. A method according to claim 10 wherein the values Nb vary according to an arithmetic sequence N1...Np and wherein the frequency F4 is determined by N1*F2 and the frequency F3 is a function of N2.

12. A method according to claim 11 wherein the value of the frequency F3 is chosen to be substantially equal to or slightly below (N1/N2)*F4.

13. A method according to claim 10 wherein the values Nb vary according to a non-arithmetic sequence and wherein two consecutive values of the sequence are divided.

14. A method according to claim 13 wherein F3 is substantially equal to or smaller than aF4 where a is the smallest value obtained in dividing two consecutive elements of the sequence.

15. A method according to claim 14 wherein the highest division rank Nb is chosen.

16. A method according to claim 10, wherein the modification of the commands of the divider and the variable-step synthesizer is simultaneous.

17. A method according to one of the above claims wherein the ratio of the reference frequency to the frequency step, Fref/ΔF, is the LCM of the sequence N1...Np.